preferably silicon nitride. Fabrication then proceeds as in the prior embodiments as discussed above."

Amend paragraph [0019] to read as follows:

"[0019] As a fourth embodiment as shown if FIGURES 4A and 4B, the FET can be made in a symmetrical rather than asymmetrical embodiment as described in the first and second embodiments with a different implant 27 in the center of the channel region as shown in FIGURE 4A. Optionally, implant 27 may include a punch-through implant. The sidewalls 11, 13 are then removed and the entire channel region is doped wither n- or p-type to provide either a less heavily net doped region adjacent the source and drain regions [29] 3, 5 if the same conductivity type dopant is used or a more heavily net doped region adjacent the source and drain regions if the opposite conductivity type dopant is used and the opposite characteristic in region 27 as shown in FIGURE 4B. Optionally, the implant in the full channel region can be performed prior to sidewall formation. Fabrication then proceeds in standard manner to complete the device."

In the claims:

Amend claim 9 as follows:

9. (Amended) A transistor which comprises:

(a) a semiconductor substrate having a surface and having a first source/drain region and a second source/drain region[s therein] spaced apart from each other and extending to said surface; and

(b) a channel region disposed in said substrate between said first and second source/drain [and drain] regions in said substrate and extending to said surface, said channel region having a

first dopant profile contacting said first source/drain region to provide a first V_T and a second dopant profile different from said first dopant profile contacting said second source/drain region to provide a second V_T different from said first V_T [having a relatively low V_T central region between said source and drain regions and relatively high V_T regions adjacent to said source and drain regions].

Amend claim 10 as follows:

10. (Amended) A transistor which comprises:

(a) a semiconductor substrate having source and drain regions therein; and

(b) a channel region between said source and drain regions in said substrate having a relatively low V_T central region between said source and drain regions and relatively high V_T regions adjacent to said source and drain regions;

[The transistor of claim 9] wherein said channel region is an implanted low V_T dopant intermediate said source and drain regions [are] and an implanted high V_T dopant adjacent said source and drain regions.

Amend claim 11 as follows:

11. (Amended) The transistor of claim 9 wherein said [channel region] first dopant profile is [an implanted] a relatively low V_T dopant implant and said second dopant profile is a selective [along said channel and a selectively implanted] relatively high V_T dopant implant [adjacent to said source region].

Cancel claims 15, 22 and 23 without prejudice.